

In the structure of Fig. 4 the microstrip, which is short-circuited, is somewhat reduced in length in order to compensate for the inductance of the bondwires to ground. The slot width was either 40, 50, or 100 μm , while the strip width remained unchanged. However, this had only little effect upon the performance, as the characteristic impedance of the slot is only weakly dependent on the slot width. According to calculations in [8], the characteristic impedance of a slotline on a substrate as in Fig. 4 increases from 51 Ω for a slot width of 40 μm to 62 Ω for 100 μm , at a frequency of 6 GHz. It is not really known how good the model of an ideal junction with perfect coupling between the slot and the striplines is, but the experimental results seem to substantiate this simple model. Also, an equivalent circuit for a slot open circuit as used in Fig. 4 is still lacking.

The increase in insertion loss below 2.0 GHz is partly due to the finite diameter of the slot open-circuit area being rather small for that frequency, and to the high-pass behavior of the slotline itself. Above 9.5 GHz it is due to the aforementioned radiation effects. Above this radiation frequency the losses decrease again.

Possible applications are that two of the structures of Fig. 4 may be used to realize a broad-band 180° phase shift. For this purpose the short circuits have to become open circuits and vice versa for one of the four transitions.

There are different ways to construct broad-band-balanced or double-balanced mixers from this transition. This can be accomplished, e.g., with one strip-slot transition in conjunction with the double junction of Fig. 2. Diodes can be put either as terminations to ports 4 and 5 (with ports 2 and 3 passively matched) or to ports 2-5.

Another way to construct a double-balanced mixer is to put an internally crossed-over diode quartet into the slotline, which is interrupted by two open circuits.

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Correction to "Efficient Minimax Design of Networks Without Using Derivatives"

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In the above paper,¹ on page 804, the logic of the flow diagram in Fig. 1 appears to be somewhat in error. The corrected flow diagram is shown here in Fig. 1.

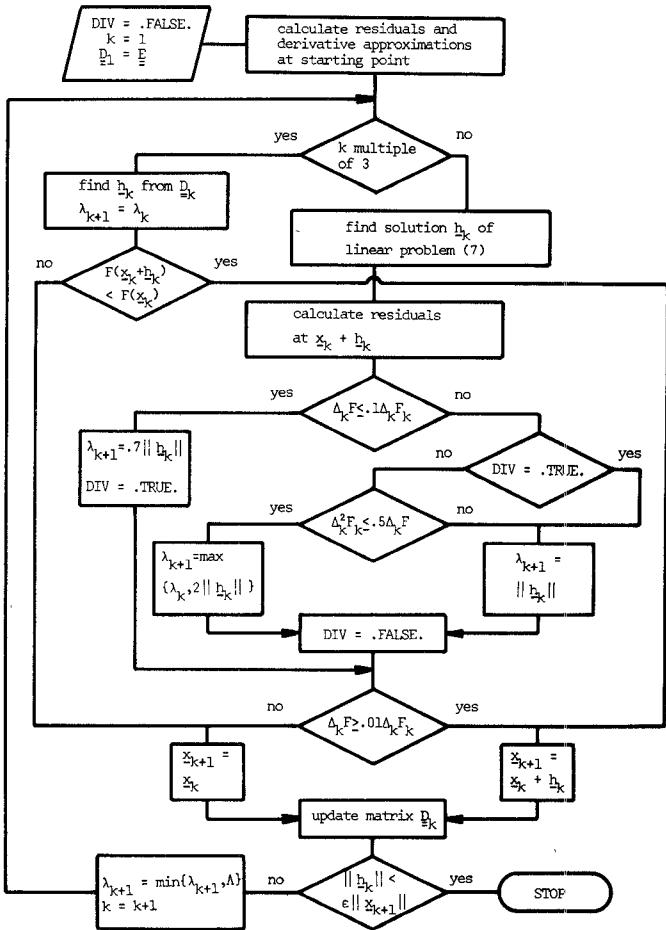


Fig. 1. Corrected flow diagram of minimax algorithm.

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